A Low Distortion Tuneable Sine Wave Oscillator

Application Note | March 20, 1998 | AN1087

One can make a low distortion tuneable oscillator by incorporating an active filter inside an AGC loop. With a control voltage V_G of 0.1 to 2V, one can obtain over a decade of tuning range, with oscillation frequencies from 200kHz to 3MHz in this particular design. Total Harmonic Distortion (THD) is -64.5dB at V_G = 1V, and is kept below -57dB over most of the tuning range. Modulation sidebands due to loop jitter are at least 50dB down over the entire tuning range, with suppression approaching 56dB for higher V_G. Linearity error for f_{OSC} vs. V_G is below 4%.

THEORY OF OPERATION

The active filter employed in this design is a state variable configuration with the EL2082 in the integrator path providing the frequency control; a circuit diagram of this filter is shown in Figure 1. The EL2082 is a current mode multiplier with low input impedance (95Ω nom) and current source output. It takes the current through the integrator resistor R_{IN}, scales it by a gain determined by V_G, then outputs the scaled signal current to the integrator capacitor C_F. In effect, we can modify the integrator time constants by adjusting V_G; the filter cutoff frequency is then given by

$$f_O = \frac{V_G}{1V} \frac{1}{2\pi(R_{IN} + 95\Omega)C_F}$$

This filter serves as the feedback network for the oscillator, a block diagram of which is shown in Figure 2. At frequency f_O, the filter phase is 0°, and if the feedback gain is ≥1, sustained oscillation will occur. To ensure startup, many oscillator designs have feedback gain >1, but then oscillation amplitude grows until nonlinearity sets in and reduces the loop gain down to 1, thus making it difficult to generate a pure sine wave. In this design, Automatic Gain Control (AGC) is used to maintain unity gain and stable oscillation amplitude. The AGC circuit consists of a 4-quadrant multiplier, which multiplies the output sine wave with itself to generate a DC and double frequency term. The high frequency term is filtered and the remaining DC voltage, which provides a measure of the output amplitude, is used to control the variable gain amplifier. This gain is continually adjusted to provide unity gain around the feedback loop.

Figure 3 shows a circuit diagram of this oscillator. The top part of the diagram is the tuneable active filter implemented using two EL2082s and a EL2444 quad op amp package. The output of this filter is fed back to its input via a unity gain buffer, obtained by connecting pins 11 and 14 of the EL4451 together. To compensate for filter losses, this output is also fed through the resistive divider R_1/R_2 into the variable gain amplifier of the EL4451. By setting the gain to just the right amount, we have unity gain in the feedback path and the necessary conditions for stable oscillation.

This adjustment is provided by an AGC, which consists of the EL4450 four quadrant multiplier and a filter to act as a RMS to DC converter. If the oscillation amplitude increases, the DC control voltage also increases to lower the gain of the EL4451 amplifier. The inverse can be said for oscillation amplitude that is too small. The loop will servo itself until the mean-square of the oscillation amplitude equals the reference voltage on pin 10 of the EL4450. This reference voltage can be changed by adjusting the potentiometer VR1.

Design Notes

Several issues were raised in this design, the first of which is the speed and stability of the AGC loop. A loop that is too slow, as was found early on, is not able to track the oscillation amplitudes; what results is a backlash phenomenon where the loop is constantly over-correcting and never finds a stable operating point. On the other hand, a loop with too much bandwidth would allow excessive feedthrough, again destabilizing itself and distorting the output. A loop bandwidth of ~16kHz has been found to be adequate for this design.

Referring to Figure 3, we see that the EL4450 provides a “pseudo” integrator in its output path; it is termed pseudo since it provides rolloff only until ~16kHz, after which it becomes a unity gain element. To continue the rolloff after 16kHz, we need an additional lowpass filter with a pole at the above frequency. Although this seems sound, we encountered loop instabilities with this implementation. By moving the pole of the lowpass filter above the “integrator zero”, the loop is stabilized.

The residual loop jitter causes another problem: modulation noise. Small variations in the loop voltage that reach the GAIN- pin of the EL4451 modulates the gain and creates Amplitude Modulation (AM) in the output waveform. Although this modulation is small, it is observable on the spectrum analyzer as sidebands around the fundamental. To reduce these sidebands we lowered the feedback into the multiplier, set by R_1 and R_2. Since the loop voltage directly modulates this feedback, by lowering the feedback we also lower the modulated components.

Another problem is the limited Q provided by the active filter network. As opposed to a crystal or LC tuned circuits, we are limited to painfully low Q's in this filter. Since $Q \neq 1$ unbalances the gain between filter stages, there is a practical limit to Q before the 2nd integrator is overdriven. Ideally we would like a high Q to reduce phase noise and to reduce the loop jitter. Unfortunately in this implementation, while Q > 1 does reduce modulation effects, it also increases

the THD due to the gain unbalance mentioned earlier. In addition, a Q > 1 also introduces clipping problems in that during startup, the oscillator can swing to large amplitudes and clip, and the AGC has no hope of recovering from such an unhappy beginning. Hence, a Q = 1 was chosen for this design to provide reliable startup and lower THD.

As the frequency of operation increases, we see peaking in the active filter due to increased phase shifts through the op amp stages. Once the peaking causes the filter gain to exceed 0dB at 0° filter phase, the AGC is no longer able to keep the feedback gain to 1, and clipping occurs in the oscillator output. For this reason it is recommended that the oscillation frequency be kept under 3.5MHz. The range of operation in this design thus lies quite close to the upper limit. For those desiring lower frequencies of operation some recommended component values are given below:

TUNING RANGE	R_{IN}	C_F	R_1	R_2	C_1	C_2
20kHz–300kHz	3K	330pF	330	240	10nF	10nF
200kHz–3MHz	3K	33pF	330	120	1nF	1nF

The current design runs on a supply of ±5V. It is possible to push the upper frequency limit to about 4MHz by operating on ±12V supplies, provided that the current limiting resistor R_Z for the LM337 is raised to 2kΩ.

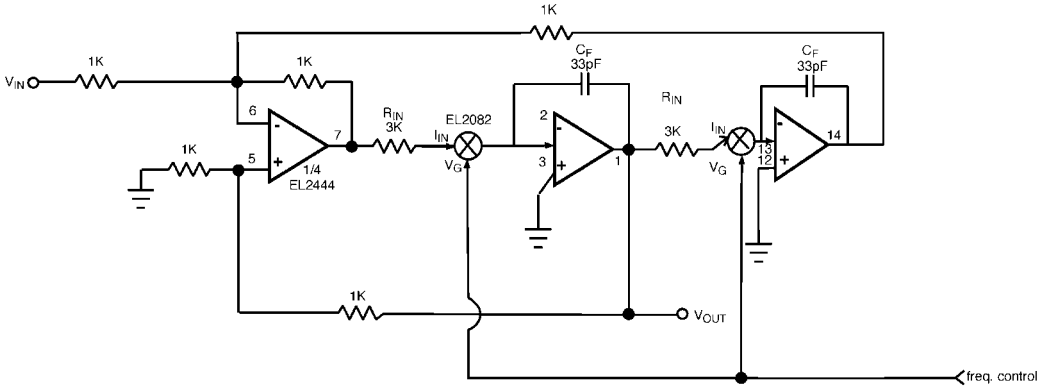

FIGURE 1.

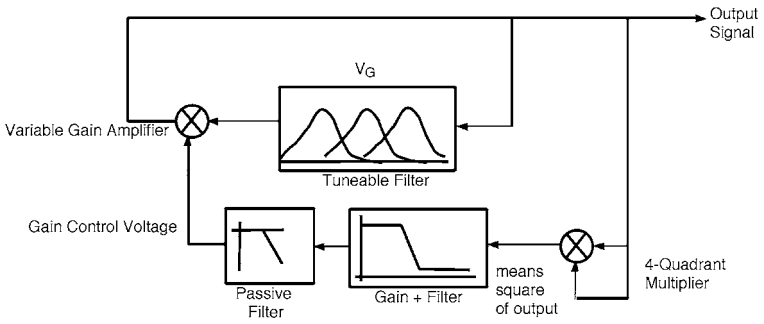

FIGURE 2.

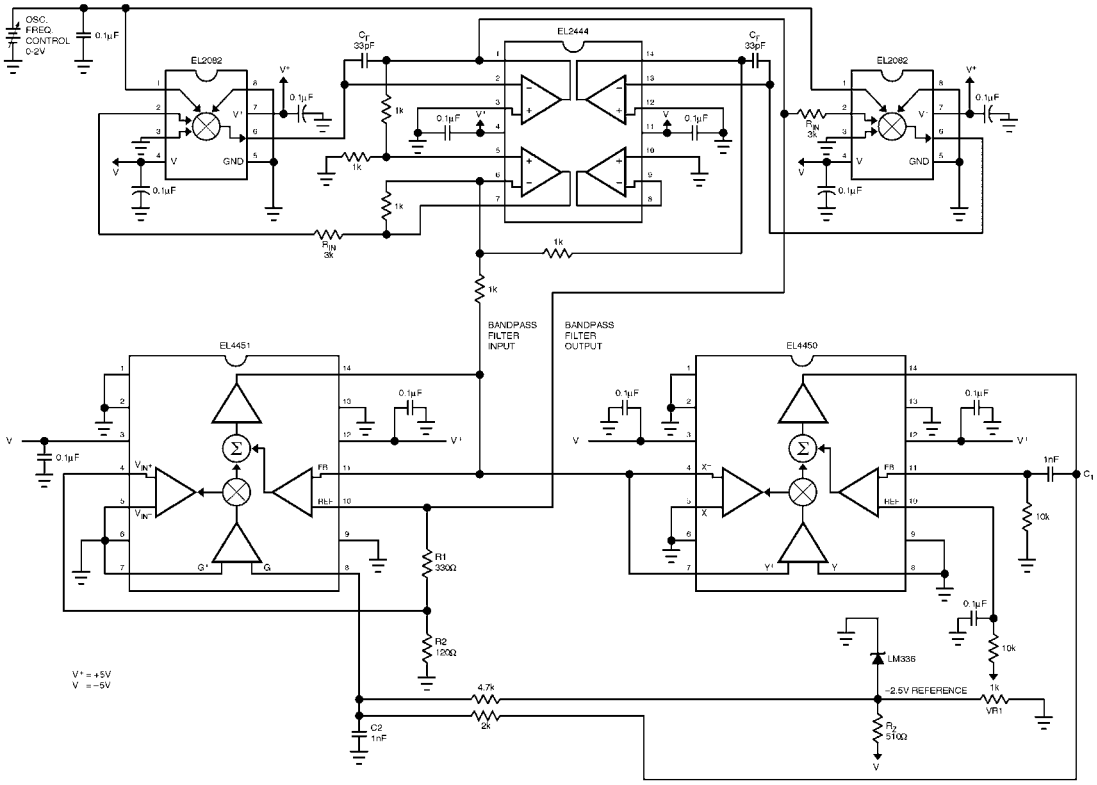

FIGURE 3.

Typical Performance Curves